A 3.9 mW 25-Electrode Reconfigured Sensor for Wearable Cardiac Monitoring System

Long Yan, *Student Member, IEEE*, Joonsung Bae, *Student Member, IEEE*, Seulki Lee, *Student Member, IEEE*, Taehwan Roh, *Student Member, IEEE*, Kiseok Song, *Student Member, IEEE*, and Hoi-Jun Yoo, *Fellow, IEEE*

***Abstract*—A low power highly sensitive Thoracic Impedance Variance (TIV) and Electrocardiogram (ECG) monitoring SoC is designed and implemented into a poultice-like plaster sensor for wearable cardiac monitoring. 0.1 Ω TIV detection is possible with a sensitivity of 3.17 V/Ω and SNR > 40 dB. This is achieved with the help of a high quality (Q-factor > 30) balanced sinusoidal current source and low noise reconfigurable readout electronics. A cm-range 13.56 MHz fabric inductor coupling is adopted to start/stop the SoC remotely. Moreover, a 5% duty-cycled Body Channel Communication (BCC) is exploited for 0.2 nJ/b 1 Mbps energy efficient external data communication. The proposed SoC occupies 5 mm × 5 mm including pads in a standard 0.18 μm 1P6M CMOS technology. It dissipates a peak power of 3.9 mW when operating in body channel receiver mode, and consumes 2.4 mW when operating in TIV and ECG detection mode. The SoC is integrated on a 15 cm × 15 cm fabric circuit board together with a flexible battery to form a compact wearable sensor. With 25 adhesive screen-printed fabric electrodes, detection of TIV and ECG at 16 different sites of the heart is possible, allowing optimal detection sites to be configured to accommodate different user dependencies.**

***Index Terms*—Body channel communication (BCC), cardiac monitoring, fabric electrode array, healthcare sensor, planar-fashionable circuit board (P-FCB), remote control, thoracic impedance variance (TIV), wearable-body sensor network (W-BSN).**

I. Introduction

PATIENT centric heart monitoring is essential because heart disease is a chronic process and a costly health problem around the world [1]. Together with Electrocardiogram (ECG) and blood pressure monitoring, the measurement of Stroke Volume (SV) and Cardiac Output (CO) [2], [3], [7], [8] play a major part in the diagnosis and therapy of pandemic diseases such as hypertension and heart failure. Since diseases of the cardiovascular system are often associated with changes of CO, this is an important measure for clinical medicine as it provides the potential for improved diagnosis of abnormalities. Invasive intra-cardiac catheterization and non-invasive Doppler ultrasound anatomy are popular methods [2], [3] in the hospital for CO evaluation. However, catheter insertion [2] into the heart has associated high risk and side effects. Alternatively, Echocardiography [3] provides a noninvasive treatment, however the equipment is typically bulky and controlled by highly skilled and experienced operators which increases treatment costs. Therefore, neither method is a convenient solution for low cost, preventative cardiac healthcare.

Recent achievements in the field of wearable healthcare sensor systems, from sensor Integrated Circuit (IC) technology, low energy bio-signal processing and wireless communication techniques, to e-textile and fabric circuit board technology in general, give opportunities to shift the healthcare paradigm towards applications of non-invasive low cost wearable healthcare. A number of wearable healthcare systems based on Wearable-Body Sensor Networks (W-BSN) have been reported to date [4]–[6]. The approaches introduced in [4] and [5] provided wireless single point ECG recording. A low-cost multi-point ECG recording was also presented in [6]. A maximum 48 points of ECG were sensed by using disposable bandage type sensors, and the measured ECG data were collected and transmitted by a W-BSN controller through an arrayed fabric inductor coupling. However, the approaches in [4]–[6] were mostly optimized for ECG signal acquisition as well as Heart Rate (HR) detection in a cost-effective and convenient way. Consequently, only the electrical activity of the heart is measured in [4]–[6]. Our goal is to provide additionally the measurement of valuable hemodynamic parameters related to the volume of blood being pumped by the heart, to enable beat-to-beat CO estimation. Since CO is the volume of blood being pumped by the heart in one minute, measurement of blood volume changes associated with bio-impedance changes in the thorax at each cardiac cycle (known as Thoracic Impedance Variance (TIV)), can directly provide important time information for CO estimation [7], [8]. Practically, the measurement of TIV is difficult to realize with low power consumption due to the requirement for high impedance (40–400 mΩ) detection sensitivity [8]. Following international safety regulations, a pure single tone sinusoidal current at 10–100 kHz applied to the patient for TIV measurements must have an amplitude less than 1 mA_{rms} [9]–[13]. As a result, the Amplitude Modulated (AM) TIV signal obtained is very small, typically several tens of μV, with a modulation depth below 3%. The low noise requirements for detecting such a small signal mean that to date only high power consuming and bulky implementations [11]–[13] have been available.

In this paper, a low power high resolution TIV and ECG monitoring SoC [14] is developed and incorporated in a compact plaster sensor form for wearable low cost cardiac healthcare. 25 electrodes operate in a reconfigurable fashion for the measurement of TIV and ECG signals at 16 different sites across the heart to enable the optimal sensing point to be selected. The

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The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: yanlong@eeinfo.kaist.ac.kr).

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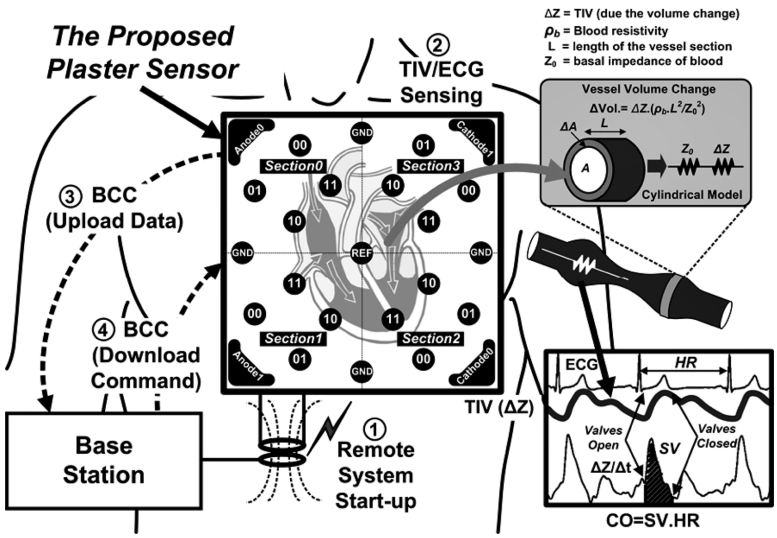

Fig. 1. Proposed wearable TIV and ECG monitoring system with poultice-like plaster sensor.

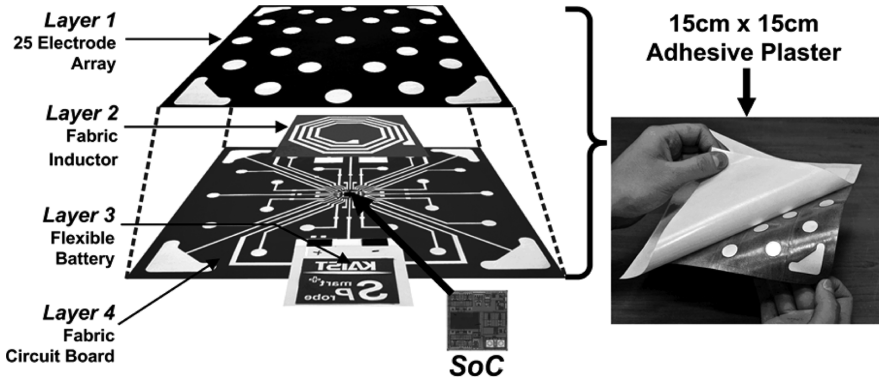

Fig. 2. Proposed wearable poultice-like plaster sensor.

proposed SoC employs a high quality ($Q > 30$) balanced sinusoidal current source together with high common-mode rejection ratio (CMRR $= 96$ dB) reconfigurable readout electronics, to measure TIV variations down to 0.1 Ω, with a sensitivity of 3.17 V/Ω and SNR > 40 dB. Two separate low power wireless communication channels are provided. A cm-range inductive coupling link is used to remotely control the system, and a 5% duty-cycled Body Channel Communication (BCC) link [15] is implemented for 0.2 nJ/b energy efficient external data communication.

This paper is organized as follows: Section II describes the proposed architecture of the wearable cardiac monitoring system and gives details of its operation. Section III discusses the detailed implementation of the SoC building blocks, including 1) Differential Sinusoidal Current Generator (DSCG), 2) high CMRR reconfigurable readout circuits, 3) remote System Start-up Module (SSM), and 4) duty-cycled Body-Channel Transceiver (BCT). Section IV shows the implementation and measurement results, and finally, Section V concludes the paper.

II. System Architecture and its Operation

Fig. 1 shows the proposed wearable TIV and ECG monitoring system based on a poultice-like plaster sensor [14], [25]. The adhesive plaster sensor is tightly attached to the chest to cover the area of the heart. The user can start and stop the system by using the cm-range inductively coupled power switch with ID verification function. When the SoC is activated, a low amplitude current ($< 300\ \mu A_{rms}$ @ 90 kHz) is injected into the body through the driving electrodes. For CO estimation, TIV signals (correlated to the distension of blood vessels at each heart beat) and ECG signals are detected through an array of 25 reconfigurable electrodes. The detected vital signs are locally processed and stored in an on-chip 20 kB SRAM memory before external transmission. When the on-chip data storage is full and the communication channel is clear, the system stops TIV and ECG recording and switches to communication mode. The BCC link is activated to upload the recorded data to a central base station, and also to download system commands if system configuration update is required. The system then resumes TIV and ECG recording.

Fig. 2 illustrates the components of the proposed adhesive sensor. The 15 cm $\times$ 15 cm 4-layer patch is screen printed with silver ink by Planar-Fashionable Circuit Board (P-FCB) technology [6], [16]–[18]. The patch consists of: Layer-1, a 25-electrode array which directly interfaces with the human chest for reconfigurable TIV and ECG measurement; Layer-2, a fabric inductor of 2.2 μH with quality factor of 9.6 for

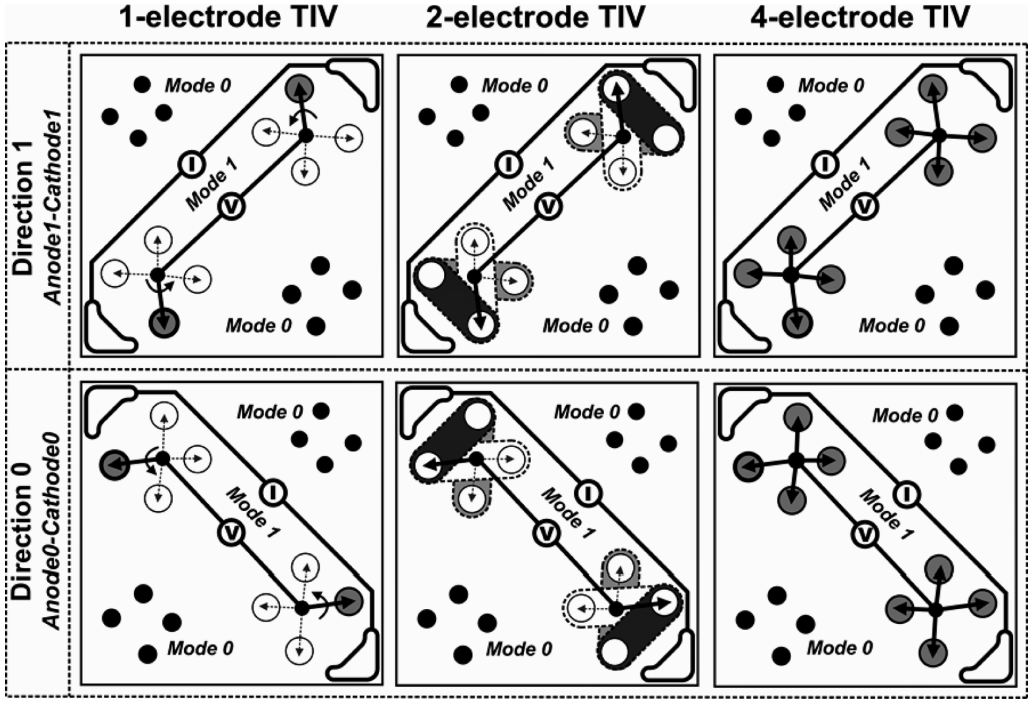

Fig. 3. Reconfigurable electrodes operation in TIV and ECG monitoring.

remote system control; Layer-3, a thin flexible battery of 1.5 V with 30 mAh capacity for continuous sensor operation; and Layer-4, a fabric circuit board on which the proposed SoC is directly wire bonded and plastic molded for protection. As shown in Fig. 1, Layer-1 has 16 voltage sensing electrodes (each 1.8 cm^2) divided into four groups, four current injection electrodes (each 3.2 cm^2) located at the corner of Layer-1, four ground electrodes (each 1.8 cm^2) and one reference electrode (1.8 cm^2) at the center of Layer-1. The 4-layer patch stacks to form a compact (thickness < 2 mm) wearable sensor device with adhesive applied on top of Layer-1 to ensure good contact to the skin.

TIV and ECG detection at 16 different sites across the heart are performed serially using the 25-electrode array in Layer-1 of Fig. 2. Fig. 3 shows the reconfigurable electrode operation for TIV measurements. After system start-up (which will be discussed in Section III-C), ECG and TIV are measured in turn through selected electrodes; for ECG the electrode-skin contact impedance is less than 120 kΩ at frequencies below 1 kHz, while for TIV measurements the electrode-skin contact impedance is typically below 300 Ω at 90 kHz. Each single measurement time period is divided into two sub-periods. During sub-period 1, ECG (Mode 0) is measured using 8 electrodes in direction 1. At the same time, TIV (Mode 1) is measured by injecting current through the outer electrodes shown in Fig. 3 and scanning through the rest of 8 measurement electrodes in turn. The reason for scanning through the measurement sites is because the TIV measurement signal is highly dependent on the location of the electrodes along the blood vessels. A higher impedance change (ΔZ) can be observed when the electrodes are located along or close to the blood vessel [11]. With reconfiguration of electrodes for TIV measurement, the optimum TIV sensing point can be determined by considering the linearity and SNR of the extracted TIV signal. In sub-periods 2, ECG (Mode 0) and TIV (Mode 1) measurements are repeated but with electrode positions changed from *direction1* to *direction0* as depicted in Fig. 3.

III. The Proposed Low Power Cardiac SoC

The overall block diagram of the proposed low power cardiac monitoring SoC is shown in Fig. 4. There are five functional blocks integrated into the SoC. They are: 1) a System Start-up Module (SSM) for remote battery control and initial BCC frequency allocation; 2) four Reconfigurable Electrode sensor Front Ends (RE-FE), with each connected to four voltage sensing electrodes to achieve reconfigurable sensing and digitization; 3) a Differential Sinusoidal Current Generator (DSCG) for high quality balanced current injection; 4) a digital module containing the FSM controller with special purpose registers (SPR), a 20 kB SRAM data storage, a 10th-order FIR filter, an 8:1 compression block [19], and a packet encoder/decoder; and 5) a duty-cycled Body-Channel Transceiver (BCT) for low energy external data communication.

The tetra-polar electrode configuration of Fig. 3 is adopted for TIV measurements to eliminate the effects of contact impedance mismatch between the two pairs of electrodes (two current injection electrodes and two voltage sensing electrodes). Fig. 5 shows the configurations used for TIV measurement. A pair of current injection electrodes (skin-contact impedance of Z_{current}) is driven by the proposed DSCG. To comply with safety regulations [9], a current magnitude of 100 $\mu A_{\mathrm{p-p}}$–350 $\mu A_{\mathrm{p-p}}$ at an exciting frequency of 90 kHz is used which is well within allowed limits. At a frequency of 90 kHz, Z_{current} is typically below 200 Ω, which minimizes loading on the DSCG, while Z_{voltage} is typically below 300 Ω, and thus contributes negligible thermal noise to the readout

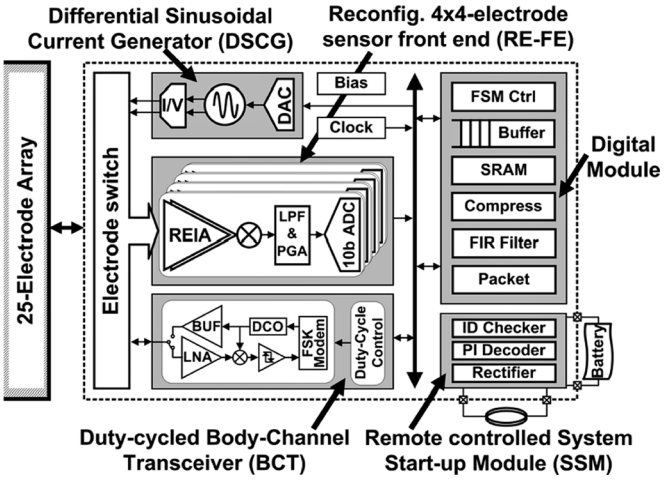

Fig. 4. Proposed low power cardiac monitoring SoC architecture.

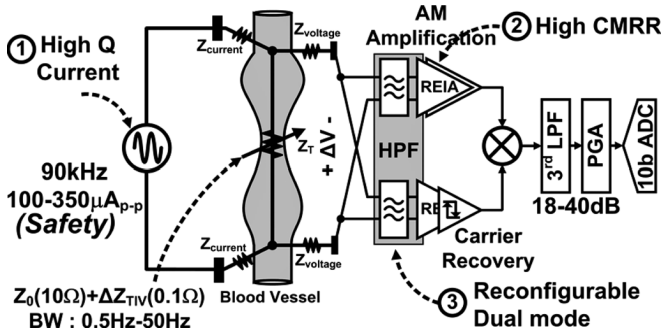

Fig. 5. TIV measurement configuration.

electronics. Furthermore, to prevent the mismatch and variation of $\mathrm{Z_{current}}$ influencing the weak TIV signal, the DSCG is designed with high output impedance (larger than 100 kΩ at 90 kHz) and the readout electronics have a correspondingly high input impedance. The balanced sinusoidal current (100 $\mu\mathrm{A_{p-p}}$–350 $\mu\mathrm{A_{p-p}}$) generated by the DSCG flows preferentially into the blood vessels in the thorax since these tissues have the lowest impedance. Preliminary tests showed that expected voltage variations with an injected current of 250 $\mu\mathrm{A_{p-p}}$ are in the range of 12.5 $\mu\mathrm{V_{p-p}}$–100 $\mu\mathrm{V_{p-p}}$ with regard to a 50 mΩ–400 mΩ impedance change. To enable detection of such weak TIV signals as well as ECG signals, a narrowband (SFDR $>$ 40 dB) high quality factor (Q-factor) current source and high CMRR ($>$ 70 dB), low noise ($\sim$ 1 $\mathrm{m\Omega_{rms}}$) readout electronics (with large signal amplification up to 80 dB) are required to achieve high TIV sensitivity (1 $\mathrm{V/\Omega}$). Moreover, the readout front end inputs must be reconfigurable to interconnect with the voltage sensing electrodes as shown in Fig. 3. The voltage readout front end requires dual mode operation for selective amplification of (alternately) TIV and ECG signals. For TIV measurement, after amplification by the reconfigurable electrode instrumentation amplifier (REIA) shown in Fig. 7, the AM modulated signal is then directly down converted by the carrier signal which has been recovered from the same pair of TIV voltage sensing electrodes. With this approach, the gain loss can be minimized due to the synchronized phase difference between the TIV signal path and the recovered carrier signal path. After AM demodulation, a third-order low-pass filter (LPF) with cutoff frequency of 50–250 Hz and a post programmable gain stage of 18–40 dB are cascaded for rejecting out-of-band noise and harmonics, and to maximize the SNR of the TIV signal before digitization.

A. Differential Sinusoidal Current Generator

The DSCG shown in Fig. 6 is one of the key building blocks in the proposed SoC which enables the high SNR TIV measurement, since a pure sinusoidal current source is difficult to realize with low power consumption and low harmonic distortion. As a result, most previous approaches were implemented either by using an external bulky sinusoidal signal generator [11], [12], or with a power consuming FPGA-based direct digital synthesizer (DDS) with low accuracy [13], [20]. To achieve both low power consumption and high signal quality, two Fully Differential Amplifiers (FDA) and an *RC* frequency selective network ($\mathrm{R} = 120\ \mathrm{k\Omega}$, $\mathrm{C} = 14$ pF) are used to generate a 90 kHz (determined by *RC* time constant $= 1/\mathrm{f_{osc}}$) balanced sinusoidal voltage signal ($\mathrm{V_{SW+}}$-$\mathrm{V_{SW-}}$) as shown in Fig. 6. The magnitude of $\mathrm{V_{SW+}}$-$\mathrm{V_{SW-}}$ can be adjusted by controlling the gate voltages of $\mathrm{M_{1,2}}$ with a 2 b DAC to modify the 3 dB corner frequency of the *RC* bridge network. The even-order harmonics are suppressed by differential signaling, and the Q-factor of the differential sinusoidal voltage signal ($\mathrm{V_{SW+}}$-$\mathrm{V_{SW-}}$) is boosted by the gain bandwidth (GBW) of the FDA, with a boosting factor of approximately $\mathrm{GBW/10f_{osc}}$. A voltage controlled current source consisting of $\mathrm{M_{3,4}}$ and $\mathrm{R_I}$ is cascaded to translate the differential voltage into a balanced current of $(\mathrm{V_{SW+}} - \mathrm{V_{SW-}})/\mathrm{R_I}$ with a constant output impedance.

The circuit topology of the gain boosted FDA used in the DSCG is also shown in Fig. 6. $\mathrm{M_{1,2}}$ of the FDA form a folded input stage, while $\mathrm{M_3}$–$\mathrm{M_6}$ boost the signal gain and create dominant poles at the gates of $\mathrm{M_7}$, $\mathrm{M_8}$. To ensure stability of the FDA, small capacitors $\mathrm{C_{1,2}}$ (200fF) are added to obtain a phase margin of 68 degrees. $\mathrm{M_{7,8}}$ not only provide a low impedance output stage via the source-follower circuit topology, but also provide common-mode feedback (CMFB) via $\mathrm{R_{1,2}}$ to control the gates of $\mathrm{M_{9,10}}$. The proposed FDA provides a GBW of 36 MHz which is sufficiently high to obtain a Q-factor greater than 30. With a power consumption of only 60 μW, the circuit provides an output impedance as low as 1.5 kΩ to effectively drive the frequency selective *RC* bridge network.

B. High CMRR Reconfigurable Readout Electronics

The reconfigurable electrode instrumentation amplifier (REIA) of Fig. 7, shared by ECG and TIV modes, enables the reconfigurable electrode operation shown in Fig. 3. The reconfigurable inputs of $\mathrm{M_{1,2}}$ are controlled by four identical switches (SE0–SE3), which provide time-multiplexed operation in ECG detection mode (Mode $= 0$), and share their inputs to achieve the variable TIV configurations shown in Fig. 3. The reconfigurable inputs provide noise advantages in both Mode 0 and Mode 1. In Mode 0, the current efficiency is increased by four, since four identical inputs share a single IA [21] and thus each utilizes all bias currents. In Mode 1, the transconductance ($\mathrm{g_m}$) of the input transistors is increased with

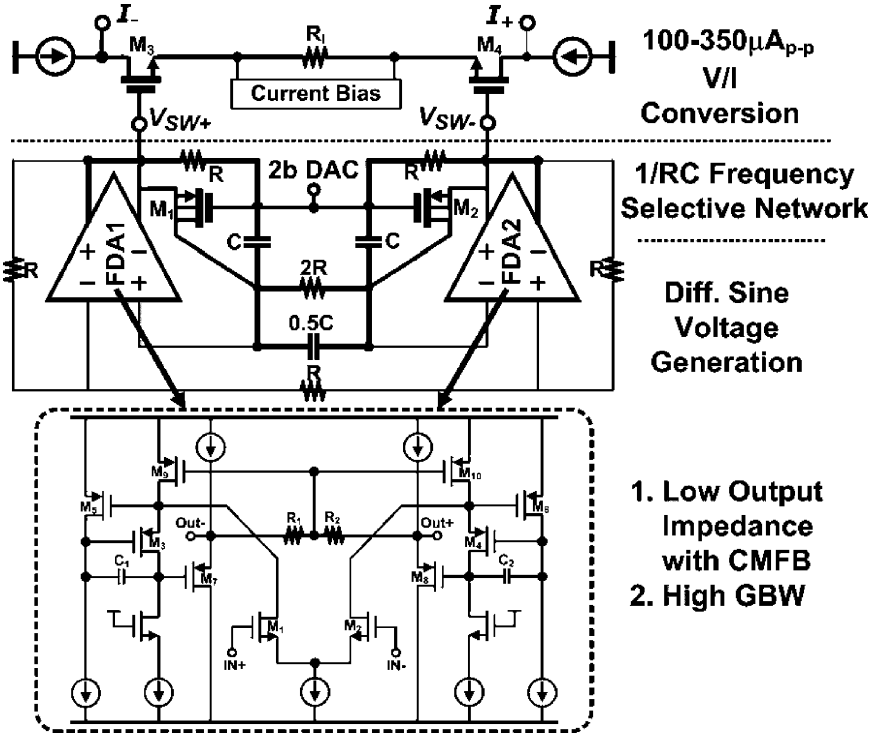

Fig. 6. Differential sinusoidal current generator (DSCG).

the increased number of input transistors switched on. This results in reduced input referred noise, which is proportional to the input g_m. In this design, the noise constraints are optimized for the single input case of REIA (58 $nV\sqrt{Hz}$); this value is reduced to 26 $nV/\sqrt{Hz}$ when all four inputs are switched on. The operating principle of the REIA is similar to the previous design introduced in [21], [22]. The differential input voltage signal is copied to R_1, which generates a current through R_1. This current signal is identically copied to R_2 to create the output voltage signal. Consequently, the gain of REIA in Fig. 7 is determined by R_2/R_1 regardless of the number of reconfigurable inputs. One of the main issues limiting the CMRR performance of the REIA is the mismatch of the differential reconfigurable inputs (M_1 and M_2). Although a large device size of $M_{1,2}$ can mitigate the V_{th} mismatch of the input transistors and improve $1/f$ noise performance, any mismatch in reconfigurable switches (SE0–SE3) pairs will also reduce the CMRR of REIA. To enhance CMRR of REIA, SE0–SE3 are located at the drain nodes of four reconfigurable inputs that maintain their drain to source voltage (V_{DS}) constant with the help of M_3–M_6. The bias currents through M_1–M_6 are fixed so as to force their gate to source voltages (V_{GS}) constant. This results in a constant DC level ($V_{DS1,2}$) shift of $V_{SG5,6}$–$V_{SG3,4}$ across the input transistors and reconfigurable switches. As a result, CMRR reduction caused by the mismatch of reconfigurable switches (SE0–SE3) can be minimized due to the immunity of drain-to-source conductance mismatch of the reconfigurable inputs.

Another feature of the REIA is the dual-mode operation to selectively amplify ECG and TIV signals with the same circuit. Fig. 8 shows the band switched filtering scheme adopted for this purpose. For simplicity, it is illustrated as single-ended although in practice the implementation is differential. Since ECG (0.5–250 Hz) and TIV (90 kHz) signals are located far apart in the frequency spectrum, a 1st-order tunable high pass filter (HPF) is located prior to REIA to minimize their crosstalk (>20 dB) and increase signal selectivity. C_H in Fig. 8 together with a pseudo-resistor (two off-state back-to-back connected pMOS devices) creates a high-pass corner of 0.4 Hz for Mode0. In Mode1, a high resistance poly resistor (R_H) of 1 MΩ is switched in to create a high-pass corner of 20 kHz for out-of-band signal rejection. The incremental resistance of the pseudo-resistor is greater than 10 GΩ for voltage differences below $\pm$400 mV, which is high enough for this application. Although the differential HPF suffers from mismatch around the 3 dB corner frequency, Monte Carlo simulations show that the CMRR remains greater than 80 dB at 60 Hz. With this band switched filtering scheme, any large DC offsets introduced from the electrodes in Mode0 are rejected by the AC coupling, while in Mode1 undesired out-of-band interferences such as 60 Hz power line disturbances are also rejected. Similarly, a switchable first-order low-pass filter (LPF) after the REIA is realized by controlling the load capacitor (C_2) of REIA. Combined with R_2 in Fig. 8, it limits the bandwidth of REIA of 1.1 kHz in Mode0 and 280 kHz in Mode1, respectively.

The rest of the analog readout signal path is shown in Fig. 9, again illustrated single ended for simplicity. A 20 dB gain stage is added after the REIA so as to post-amplify TIV signals which are in the range of a few mV, before frequency down conversion. After the recovered carrier signal is multiplied with the AM modulated TIV signal for demodulation, a 50–250 Hz LPF is cascaded to remove 2nd order harmonics of the carrier signal and to filter out-of-band noise, including residual offsets from the REIA. Although the LPF removes high frequency noise,

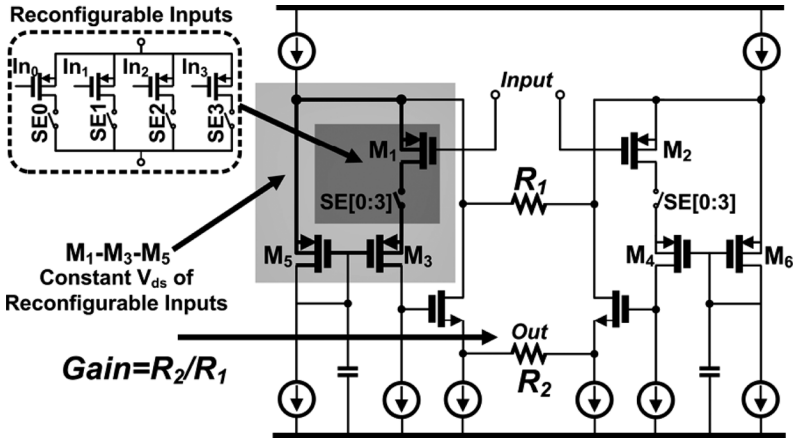

Fig. 7. Reconfigurable electrode instrumentation amplifier (REIA).

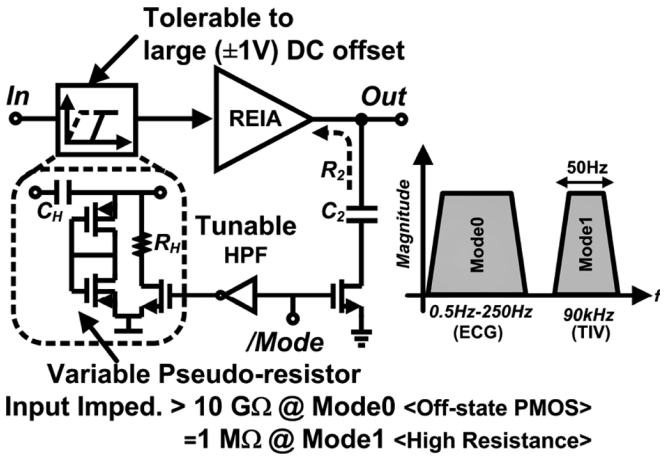

Fig. 8. Dual-mode operation with band-switched filtering.

interference, and modulated residual offsets from the previous gain stage effectively, the respiration-correlated artifacts still remain in the frequency band 0.05–0.5 Hz after frequency down conversion. If these are not removed before post amplification, large signal distortion will occur before digitization. As a result, the third gain stage is implemented with a bandpass characteristic, with programmable gain of 18–40 dB for SNR enhancement. To minimize the degradation of SNR while providing accurate gain, a continuous-time programmable gain amplifier (PGA) as proposed in [23] is implemented with MIM capacitors (C_1 and C_2). Two diode-connected pMOS transistors in series act as pseudo resistors to reduce distortion for large output signals. Combined with C_2 (100 fF–1.26 pF), they create a 0.3–3 Hz high-pass corner which attenuates respiration artifacts and thus minimizes distortion of the desired TIV signal. The total gain used for the TIV channel can be set to 66 dB, 74 dB, 80 dB, or 88 dB. The TIV signal from the optimal electrode detection sites will provide maximum SNR. In this design, we achieve optimal performance by ensuring the TIV signal at the PGA output is within the voltage range 37.5–562.5 mV with respect to an ADC reference voltage of 600 mV. The lower limit is chosen to ensure SNR larger than 20 dB and the upper limit is chosen to ensure THD below 2%. The detection is realized in the digital domain by simply comparing the ADC output with the reference voltage criteria.

C. Remote System Start-Up Module

The proposed wearable cardiac monitoring system starts with a remote 8 b ID check. The System Start-up Module (SSM) of Fig. 10 operates via cm-range inductive coupling to realize remote system control. The operation consists of four steps. In *Step 1,* the remote controller in the base station provides a continuous wave at 13.56 MHz through fabric inductor coupling [6]. In *Step 2*, a CMOS rectifier in the SSM generates a short period (10 μs) Power-on-Reset (PoR) trigger signal, which is used to modulate the receiving coil of SSM so that backscatters the PoR to the remote controller. In *Step 3*, the remote controller transmits an ID packet at 0.8 kb/s, including the 8 b ID code which is pulse interval (PI) encoded. Finally in *Step 4*, the PI decoder in SSM decodes the data packet and verifiers its ID code asynchronously; if the ID is verified the flexible battery will activate the SoC. With this scheme, user-friendly system start-up is realized remotely without using any bulky mechanical power switch.

Fig. 11 shows the asynchronous PI-decoding scheme adopted in SSM. Once the CMOS rectifier receives the data packet from the remote controller and generates the PI-encoded (PIE) envelope of Fig. 11 with a symbol period of 1.25 ms, this signal is fed into the PI-decoder to decode the data without requiring an on-chip clock. Each symbol of the PIE envelope starts with '0' and finishes with '1' to separate each symbol. The data is encoded between the start and stop bits as a 2 b digital code (ex, 0001 for *data* '0' and 0111 for *data* '1'). *REF* and *ID Data* are generated with different slopes as shown in the measurement results of Fig. 11. *REF* as a threshold signal is created by charging a 4 pF MIM capacitor (2C) by turning on the current switch of M_1 for a single symbol period, while the *ID data* is generated by charging a 2 pF MIM capacitor (C) via M_2 which is controlled by the PIE envelope. To match the charging times, the supply current is designed to be identical to the regulated current mirror circuit. Each data bit is identified at each negative edge of the symbol by a comparison between *ID data* and *REF* signal. At the same time, reset of *ID data* is accomplished by discharging the 2 pF MIM capacitor (C). The measurement

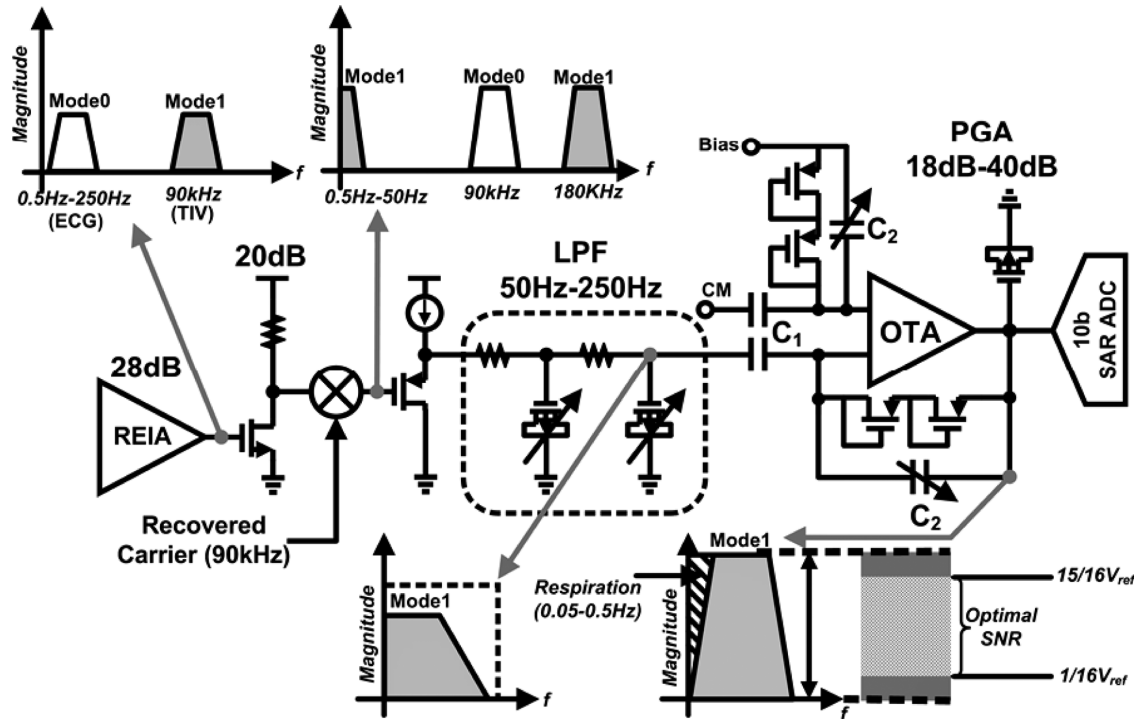

Fig. 9. Post processing analog readout signal path.

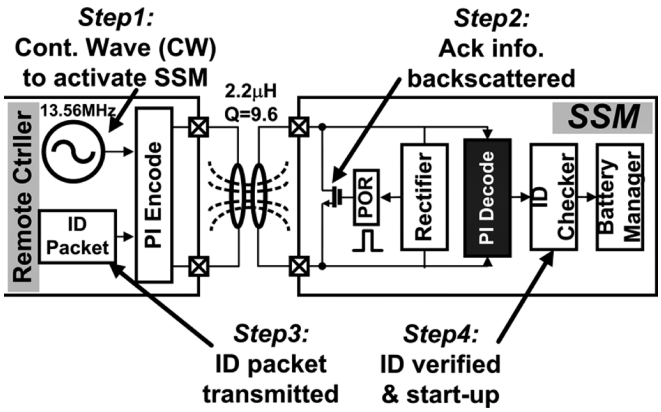

Fig. 10. Remote system start-up module (SSM).

results in Fig. 11 show a 13.56 MHz ASK modulated 8 b ID code being decoded asynchronously by the SSM. In this design, the remote controller sends a continuous wave (13.56 MHz) for 800 μs before sending the desired data, in order to create a negative edge at the start of the data packet. Once the ID is decoded, an on-chip preprogrammed reference 8 b code (00100111) is used to authenticate the decoded ID with 8 b-XOR gates. Then, the battery is turned on to start up the SoC if the received ID is identical to reference code.

D. Duty-Cycled Body-Channel Transceiver

The architecture of the FSK BCT is shown in Fig. 12. To minimize path loss and interference [24], 20–40 MHz is used as a communication channel with four separate bands. Each band of 5 MHz gives a data rate of 1 Mbps, enabling a low power, high duty-cycled BCC. TIV and ECG signals are sampled at 500 sample/s with 10 b resolution and compressed 8:1 before being stored in on-chip 20 kB SRAM. This data is measured and stored continuously for 16 s before measurement stops and the data is transmitted. During the measurement period, the BCT periodically operates in RX mode for 0.1 s every 4 s to update clear channel assessment for interference. As a result, 5% duty cycled BCT operation is achieved. The BCT in [15] continuously consumes up to 2.3 mW power excluding the power dissipation of external components; such continuous operation will reduce the battery lifetime or even collapse the battery in this application. Moreover, the direct-switching FSK modulator based on two identical PLLs proposed in [15] requires an external 20 MHz X-tal, and takes more than 1 ms for frequency stabilization. In this design, a FSK transmitter based on a digitally-controlled *LC* oscillator (LC-DCO) with 8 b capacitor bank is proposed, with a duty-cycled power gating technique enabling fast wake up (within 1 μs) and allowing removal of the external X-tal.

Fig. 13 shows the LC-DCO based FSK modulator for our 5% duty-cycled BCT. Two on-chip inductors (each of 14 nH) with an 8 b capacitor bank are used to generate an oscillation frequency between 500 MHz to 780 MHz, while consuming only 1 mA bias current from a 1.5 V supply voltage. 20–40 MHz FSK signals are produced using an integer frequency divider (1/16–1/32). The generated frequency shows a phase noise better than 120 dBC at 1 MHz offset, and provides maximum 200 ppm frequency stability over a temperature variation of 70 °C. On the receiver side, a 20 dB gain stage is cascaded after the LNA [15] before direct down conversion to improve the noise figure by 3 dB. This enables robust operation even with a 10% frequency offset between transmitter and receiver. Although the receiver consumes 3.2 mW in operation, the average

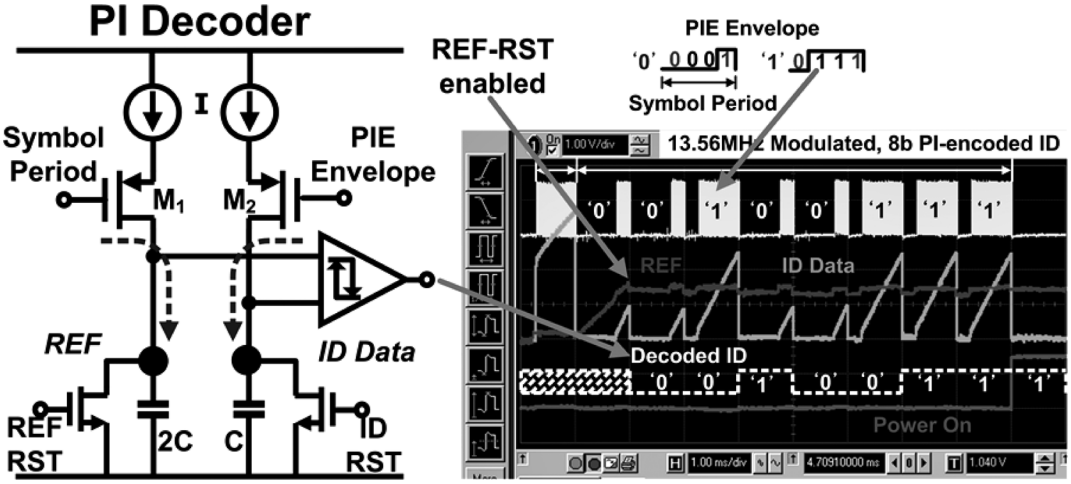

Fig. 11. Asynchronous PI-decoding in SSM with measurement results.

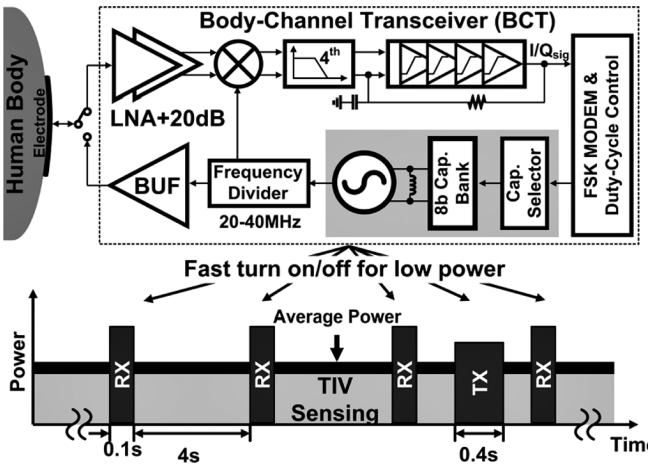

Fig. 12. Duty-cycled body-channel transceiver (BCT).

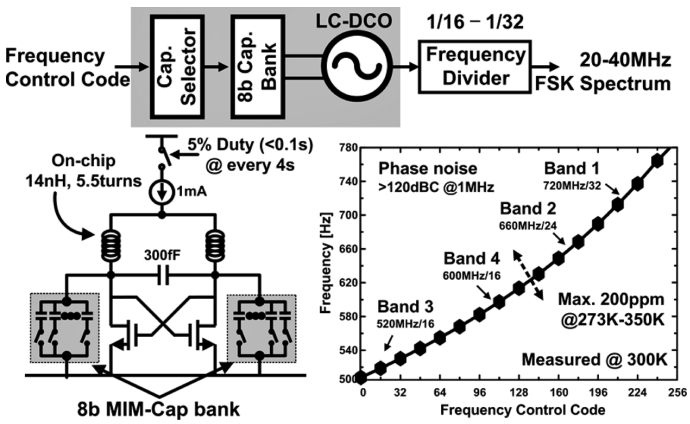

Fig. 13. LC-DCO based FSK modulator and its measurements of frequency sensitivity.

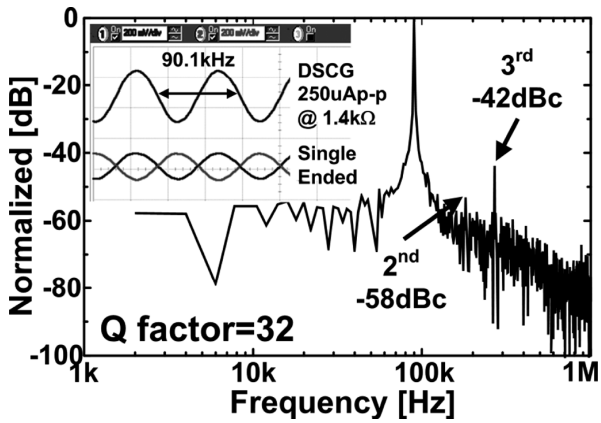

Fig. 14. Output spectrum of DSCG when it drives 1.4 kΩ load impedance with 250 μA_{p-p} current.

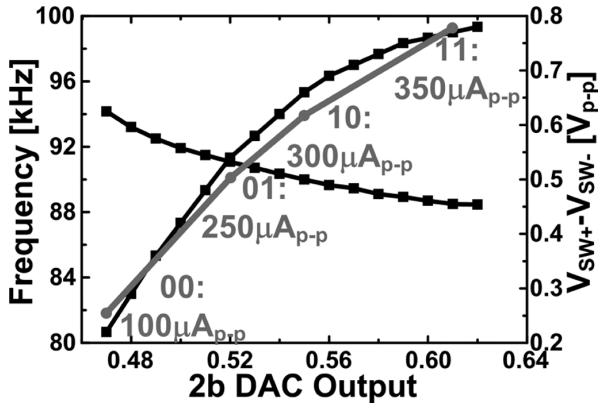

Fig. 15. Frequency change in DSCG with output current of 110 μA_{p-p}–350 μA_{p-p}.

power consumption of BCT can be reduced to 200 $\mu W_{average}$ when the 5% duty-cycled power gating technique is applied.

IV. Implementation and Measurement Results

The poultice-like plaster sensor (Fig. 2) for wearable cardiac monitoring is implemented using P-FCB technology. It was fabricated as a compact adhesive plaster sensor of 15 cm × 15 cm with thickness < 2 mm. Fig. 14 shows the output spectrum of the DSCG when driving a 1.4 kΩ load impedance with a 250 μA_{p-p} balanced sinusoidal current. The second-order harmonic is suppressed down to −58 dBc, which is a 40% enhancement compared with the single-ended version. The third-order harmonic of the DSCG is at −42 dBc, resulting

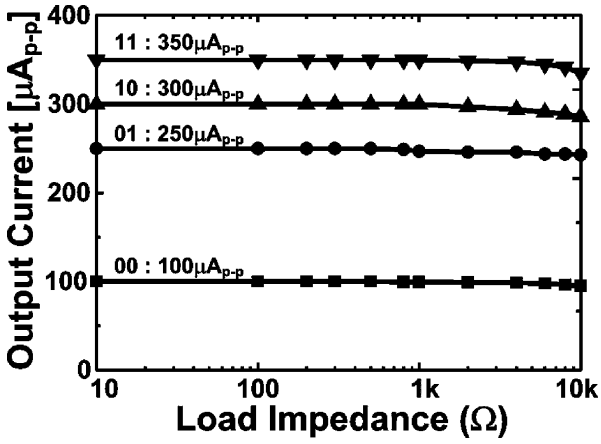

Fig. 16. Output current stability of DSCG with load impedance variation.

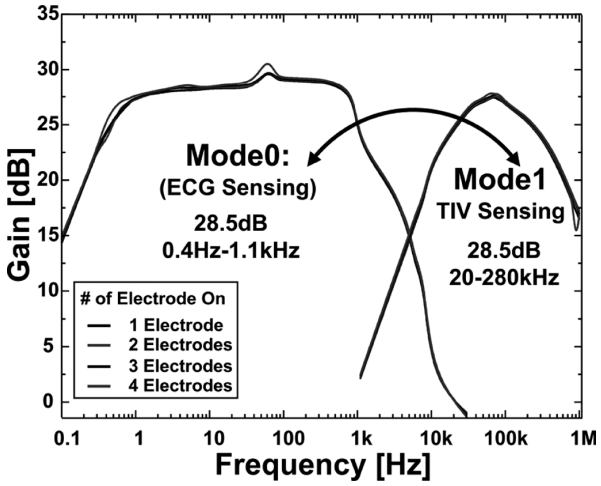

Fig. 17. Measured gain curve for dual-band operation of REIA.

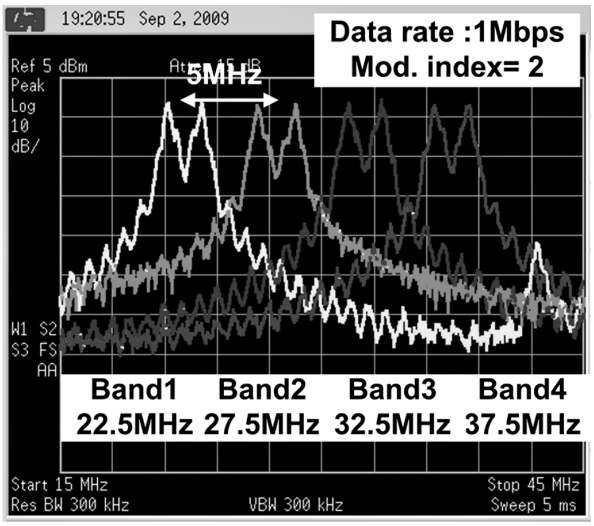

Fig. 18. Four-band FSK output spectrum of BCT at TX mode.

in total harmonic distortion (THD) of 0.81% and quality factor of 32. The variable output current of DSCG was also tested with 2 b DAC control. As shown in Fig. 15, the 2 b DAC output of Fig. 6 adjusts the gate voltage (V_{SW+}-V_{SW-}) of $M_{3,4}$ in

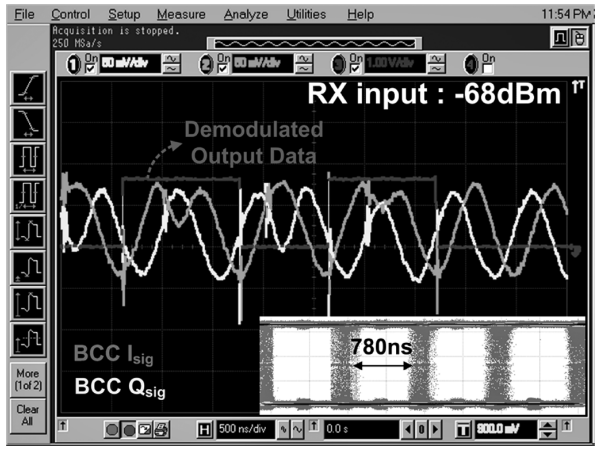

Fig. 19. 1 Mbps baseband I/Q signals and eye diagram of BCT at RX mode.

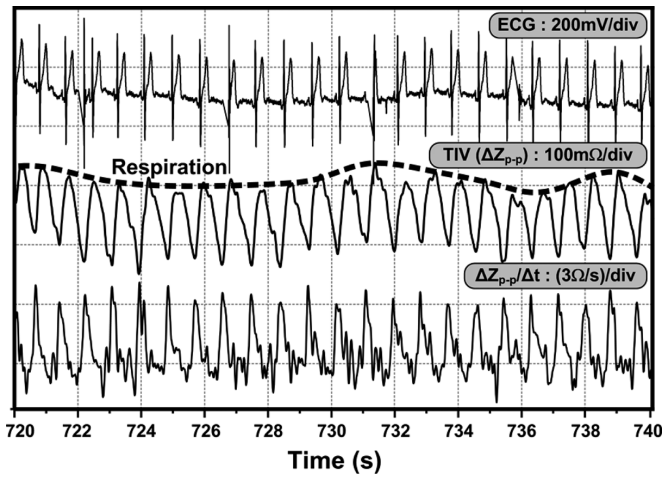

Fig. 20. Measured TIV and ECG waveforms.

the DSCG, resulting in peak-to-peak sinusoidal voltages of 0.22 V_{p-p}–0.78 V_{p-p}. These voltage signals are converted to differential current signals of 100 μA_{p-p}–350 μA_{p-p}. A maximum frequency variation of 6 kHz due to the variation in current is observed during the measurement. However, the TIV detection shown in Fig. 5 recovers the carrier signal from the AM voltage signal directly, and thus ensures synchronization between the carrier signal for demodulation and the AM modulated TIV signal. To verify the stability of DSCG output current, the load impedance was changed from 10 Ω to 10 kΩ while providing a variable current of 100 μA_{p-p}–350 μA_{p-p} as shown in Fig. 16. A maximum current variation of 1% is measured with a load impedance below 5.6 kΩ, stable enough to drive a pair of current electrodes. Fig. 17 illustrates the measured gain curve of REIA (Fig. 7) for dual-band operation. 28.5 dB gain in Mode0 and 27.8 dB gain in Mode1 are measured respectively, regardless of the number of electrodes switched on. This band switching ensures that the ECG signal band (0.4–1.1 kHz) and TIV signal band (20–280 kHz) are isolated by more than 20 dB, which enhances signal selectivity.

Fig. 18 shows the 4-band FSK output spectrum of body channel transmitter with a data rate of 1 Mbps and modulation index of 2. Four BCC bands are located in the 20–40 MHz

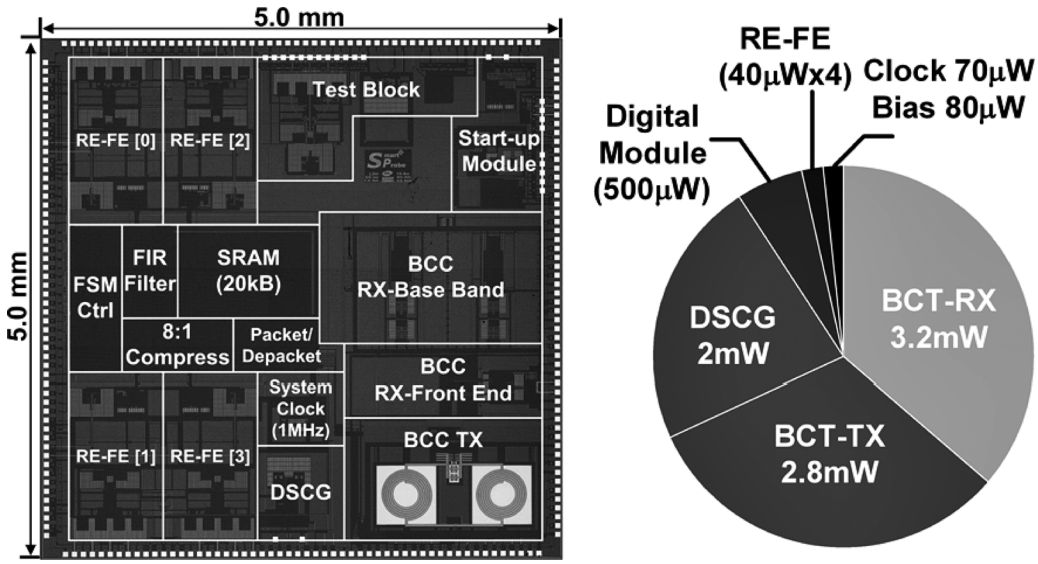

Fig. 21. Chip micrograph and its power breakdown.

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED SOC

Process	UMC 0.18μm 1P6M CMOS		**RE-FE** (40μW x 4)	Sampling	0.25k-2kSamples/s
Die Size	5.0 x 5.0 mm^2 (including pads)			Gain	65.8dB-86.2dB
Power	Supply Voltage	1.2V~1.5V		Bandwidth (3dB)	0.4Hz-1.1kHz 20kHz-280kHz
	Max. 3.9mW (BCT activated) 2.4mW (TIV detection)			Input Noise	<1mΩ/√Hz
Digital Module (500μW)	SRAM (20kB)	64kHz		Electrode Offset Tolerance	> ±1V
	Compress (8:1)			THD	TIV/ECG: 1.6%/1% @ 450mV$_{p-p}$ Output
	10th-FIR			CMRR	TIV : 91dB ECG : 78dB
	Packet En/Decoder	1MHz	**BCT** RX 3.2mW TX 2.8mW @ P_{out}=-6dBm	Channel	20MHz-40MHz (4ch)
DSCG (2mW)	Injection Current (90kHz)	100μA$_{p-p}$-350μA$_{p-p}$ (4-step)		Data Rate	1Mbps (FSK)
	Sensitivity	3.17V/Ω		Sensitivity	-75dBm@10^{-6} BER
	THD	<1% @ 250μA$_{p-p}$		Interference Rejection	Listen Before Talk
				Wake-up	<1μs

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUS WORKS

	J.Yoo JSSC'10 [6]	M-C. Cho ISCAS'09 [11]	R.G. Landaeta, TBME'08 [12]	This Work
Subject	ECG @ Chest	Impedance @ forearm	Impedance @ Leg	ECG+TIV @ Chest
Impedance Sensitivity	—	45mΩ 21V/Ω	500mΩ 610mV/Ω	100mΩ 3.17V/Ω
Injection current	—	1mA$_{p-p}$, 100kHz	1mA$_{p-p}$, 10kHz	100-350μA$_{p-p}$, 90kHz
#of Point	Max. 48 points	Max. 12	4 points	Max. 16-TIVs Max. 16-ECGs
Communication	13.56MHz inductive	Wireline	Wireline	13.56MHz Inductive 20-40MHz BCC
Network Coverage	Chest Area	—	—	Body Area
Power Consumption	12μW(sensor) 5.4mW(Ctrl.)	>500mW	—	(Max.) 3.9mW (TIV) 2.4mW
Integration level	Bandage & Chest band	Bread board	PCB	4-layer poultice-like plaster
Technology	0.18μm CMOS	Off-the-Shelf	Off-the Shelf	0.18μm CMOS

spectrum (at center frequencies of 22.5 MHz, 27.5 MHz, 32.5 MHz, and 37.5 MHz). The transmitted FSK spectrum is attenuated down to −68 dBm (considering the pass loss of the body channel) to measure receiver performance. Fig. 19 shows the baseband I/Q signals and eye diagram of the demodulated bit stream at 1 Mbps data rate. A maximum eye open of 78% is measured with a 1 Mbps data rate, which drops to 71% when the receiver input signal is further attenuated from −68 dBm to −75 dBm.

Fig. 20 shows the recorded ECG and TIV signals. A long-term (20 seconds) monitoring test is performed with the subject sitting on a chair so as to minimize artifact related to motion and respiration. A TIV of 0.1 Ω is detected with a two-electrode configuration in direction1 (Fig.3), an injection current of 250 μA_{p-p} and 74 dB amplification of RE-FE. This results in a TIV detection sensitivity of 1.48 V/Ω; the sensitivity can be increased to 3.17 V/Ω with an injection current of 350 μA_{p-p} and 80 dB amplification of RE-FE. From Fig. 20, the respiration signal is estimated at 18% of TIV signal. With HR extracted from the ECG trace and derivative ($\sim 3\ \Omega/s$) of TIV, a theoretical average CO can be estimated from the equation depicted in Fig. 1 [8].

The proposed SoC is fabricated in a 0.18 μm standard 1P6M CMOS process. It occupies 5 mm × 5 mm chip area

including pads as shown in Fig. 21. The peak power consumption is 3.9 mW for the SoC operating in body channel receiver mode, and the average power consumption is 2.4 mW for the SoC operating in reconfigurable TIV and ECG detection mode. Table I summarizes the performance of the proposed SoC. A flexible battery of 1.5 V and 30 mAh is used to supply the power to the SoC. All circuits of the SoC are designed to operate down to a 1.2 V supply voltage. The digital module, containing 20 kB SRAM memory, 8:1 data compressor, 10th-order FIR filter, operates at 64 kHz and consumes 220 μW, while the packet encoder/decoder operates at 1 Mbps and dissipates 280 μW. The DSCG consumes 2 mW while providing a four-step controllable balanced sinusoidal current of 100 μA_{p-p}–350 μA_{p-p} with THD below 1%. Four identical RE-FE stages consume 160 μW, each RE-FE providing a variable gain of 65.8–86.2 dB and input referred noise density of 58 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The achieved noise density equates to an impedance noise level below 1 $\mathrm{m}\Omega/\sqrt{\mathrm{Hz}}$, which guarantees SNR of TIV larger than 40 dB. The CMRR values for ECG and TIV channels are 78 dB and 91 dB, respectively. The BCT consumes 3.2 mW when operating in receiver mode, and dissipates 2.8 mW when operating in transmitter mode. In practice, the BCT is 5% duty cycled to achieve an average power consumption of 200 μW_{average}. For immunity to interference, the BCT operates using Listen-Before-Talk (LBT) to select a clear channel from one of the four BCC bands located between 20 MHz–40 MHz. The maximum sensitivity of BCT is -75 dBm with a data rate of 1 Mbps, which is a 7 dB improvement compared with [15], and thus allows the BCT to cover the whole body area distance. Table II summarizes the performance compared to previous work. The proposed 4-layer compact plaster sensor detects ECG and TIV signals concurrently with 16 different electrode configurations. The maximum impedance detection sensitivity is 3.17 V/Ω which is more sensitive than [12] by 5 times, and consumes only 2.4 mW which is far lower than [6], [11]. Moreover, two versatile wireless communication channels are provided for W-BSN either by using cm-range 13.56 MHz inductive coupling, or 20–40 MHz BCC.

V. Conclusion

A low power, high resolution TIV and ECG monitoring SoC is designed for wearable, low cost cardiac healthcare. 0.1 Ω TIV detection is possible with a detection sensitivity of 3.17 V/Ω and SNR $>$ 40 dB. This is achieved using a 100 μA_{p-p}–350 μA_{p-p} high quality (Q-factor $>$ 30) balanced sinusoidal current source and reconfigurable high CMRR ($>$ 90 dB) readout electronics. A 5% duty-cycled BCT is designed with 0.2 nJ/b energy efficiency and -75 dBm sensitivity to communicate with the base station located in any arbitrary position on the body. The proposed SoC occupies 5 mm $\times$ 5 mm including pads in a standard 0.18 μm 1P6M CMOS technology, and it is incorporated into a 15 mm $\times$ 15 cm compact poultice-like plaster. With the help of SSM, remote activation and control of the sensor is possible by using cm-range 13.56 MHz fabric inductor coupling. The proposed sensor dissipates a peak power of 3.9 mW when operating in body channel receiver mode and consumes 2.4 mW when operating in TIV and ECG detection modes. With the proposed wearable sensor, personal, low cost, and convenient cardiac healthcare is possible.

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Long Yan (S'07) received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007 and 2009, respectively, where he is currently pursuing the Ph.D. degree.

As a chief researcher at the Semiconductor System Laboratory in KAIST, he has worked on developing low power FSK transceivers for body channel communication and low noise, wirelessly powered patch sensors for wearable body sensor network. His current research interests include energy-efficient wearable healthcare sensor system, low power body channel transceiver, power management in biomedical micro-system.

Joonsung Bae (S'07) received the B.S. and M.S. degree in electrical engineering from the KAIST, Daejeon, Korea, in 2007 and 2009, respectively, where he is currently working toward the Ph.D. degree.

He has worked on developing a transceiver for high speed and low power on-chip global interconnects. He also engaged in developing low energy wireless CMOS transceivers for communicating among wearable and implantable devices. His current research interests include low energy transceiver design for body area networks and body coupled electrical field communications.

Seulki Lee (S'07) received the B.S. and M.S. degrees, both in electrical engineering, from KAIST, Daejeon, Korea, in 2007 and 2009, respectively, where she is currently working toward the Ph.D. degree, also in electrical engineering.

Her current research interests include low energy transceiver design for near-field communication based wearable body sensor network application.

Taehwan Roh (S'09) received the B.S. degree in electrical engineering from KAIST, Daejeon, Korea, in 2009, where he is currently working toward the M.S. degree.

His current research interests include developing a low-power wearable healthcare platform and customized bio-signal processor.

Kiseok Song (S'09) received the B.S. degree in electrical engineering from KAIST, Daejeon, Korea, in 2009, where he is currently working toward the M.S. degree.

His current research interests include developing a wirelessly powered stimulator. He is also interested in body channel analysis for electrical field coupled communication.

Hoi-Jun Yoo (M'95–SM'04–F'08) graduated from the Electronic Department of Seoul National University, Seoul, Korea, in 1983 and received the M.S. and Ph.D. degrees in electrical engineering from KAIST, Daejeon, Korea, in 1985 and 1988, respectively. His Ph.D. work concerned the fabrication process for GaAs vertical optoelectronic integrated circuits.

From 1988 to 1990, he was with Bell Communications Research, Red Bank, NJ, where he invented the two-dimensional phase-locked VCSEL array, the front-surface-emitting laser, and the high-speed lateral HBT. In 1991, he became a manager of the DRAM design group at Hyundai Electronics and designed a family of fast-1 M DRAMs to 256 M synchronous DRAMs. In 1998, he joined the faculty of the Department of Electrical Engineering at KAIST and now is a full Professor. From 2001 to 2005, he was the director of System Integration and IP Authoring Research Center (SIPAC), funded by Korean Government to promote worldwide IP authoring and its SOC application. From 2003 to 2005, he was the full time Advisor to Minister of Korea Ministry of Information and Communication and National Project Manager for SoC and Computer. In 2007, he founded System Design Innovation & Application Research Center (SDIA) at KAIST to research and to develop SoCs for intelligent robots, wearable computers and bio systems. His current interests are high-speed and low-power Network on Chips, 3-D graphics, Body Area Networks, biomedical devices and circuits, and memory circuits and systems. He is the author of the books *DRAM Design* (Hongleung, 1996; in Korean), *High Performance DRAM* (Sigma, 1999; in Korean), *Low-Power NoC for High-Performance SoC Design* (CRC Press, 2008), and chapters of *Networks on Chips* (Morgan Kaufmann, 2006), chapters of *Embedded Memories for Nano-Scale VLSIs* (Springer, 2009), and chapters of *Circuits at the Nanoscale* (CRC Press, 2009).

Dr. Yoo received the Electronic Industrial Association of Korea Award for his contribution to DRAM technology in 1994, the Hynix Development Award in 1995, the Design Award of ASP-DAC in 2001, the Korea Semiconductor Industry Association Award in 2002, the KAIST Best Research Award in 2007, the Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Awards in 2005, 2006, and 2007, and the DAC/ISSCC Student Design Contests Award in 2007 and 2008. He is an IEEE fellow and serving as an Executive Committee Member and the Far East Chair for IEEE ISSCC, and a Steering Committee Member of IEEE A-SSCC. He was the Technical Program Committee Chair of A-SSCC 2008.